What is claimed:

1. A semiconductor device comprising:

a protective insulation layer;

a pad opening section provided in the protective insulation layer;

a wiring layer which the pad opening section reaches; and

a wiring layer provided at a level lower than the wiring layer which the pad opening section reaches,

wherein the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

2. A semiconductor device according to claim 1, wherein the wiring layer which the pad opening section reaches is composed of one layer.

3. A semiconductor device according to claim 1, wherein the wiring layer which the pad opening section reaches is composed of two layers.

4. A semiconductor device according to claim 1, wherein the wiring layer which the pad opening section reaches has a thickness that is greater than that of the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches.

5. A semiconductor device comprising:

a first wiring layer formed above a semiconductor layer through a first interlayer insulation layer;

a second wiring layer that provides a pad section formed above the first wiring layer through a second interlayer insulation layer;

a protective insulation layer formed above the second wiring layer and the second interlayer insulation layer; and

a pad opening section provided in the protective insulation layer,

wherein an upper surface of the first interlayer insulation layer includes a first region where the protective insulation layer is formed vertically thereabove, and

the first wiring layer is formed on the first region.

6. A semiconductor device according to claim 5, wherein

the upper surface of the first interlayer insulation layer further comprises a second region where the pad opening section is formed vertically thereabove, and at least part of the second interlayer insulation layer is formed on the second region.

7. A semiconductor device according to claim 5, wherein the first wiring layer includes a plurality of wiring layers in the same layer, and the plurality of wiring layers are formed on the first region.

8. A method for manufacturing a semiconductor device, the method comprising the steps of:

(a) forming a wiring layer on an interlayer insulation layer;

(b) forming a protective insulation layer on the interlayer insulation layer and the wiring layer; and

(c) forming a pad opening section in the protective insulation layer, which reaches the wiring layer,

wherein the semiconductor device includes a wiring layer provided at a level lower than the wiring layer to which the pad opening section reaches,

wherein the pad opening section is formed such that the wiring layer provided at a level lower than the wiring layer to which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

9. A method for manufacturing a semiconductor device according to claim 8, wherein the wiring layer which the pad opening section reaches is composed of one layer.

10. A method for manufacturing a semiconductor device according to claim 8, wherein the wiring layer which the pad opening section reaches is composed of two layers.

11. A method for manufacturing a semiconductor device according to claim 8, wherein the wiring layer which the pad opening section reaches has a thickness that is greater than that of the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches.

12. A semiconductor device according to claim 5, wherein the first wiring layer is only formed on the first region.

13. A semiconductor device according to claim 6, wherein the first wiring layer is only formed on the first region and the second interlayer insulating layer is formed over the entire second region.

14. A semiconductor device as in claim 13, wherein a portion of the second interlayer insulating layer is formed over the first region.

15. A semiconductor device as in claim 5, further comprising:

a third wiring layer positioned between the first wiring layer and the second wiring layer; and

a third interlayer insulation layer positioned between the first interlayer insulation layer and the second interlayer insulation layer.

16. A semiconductor device as in claim 15, wherein the third wiring layer is connected to the first wiring layer through a plurality of first plugs and the third wiring layer is connected to the second wiring layer through a plurality of second plugs, and the first plugs and the second plugs are positioned to be offset from each other in a vertical direction.

17. A method for manufacturing a semiconductor device, comprising:

forming a lower level wiring layer;

forming an lower level interlayer dielectric layer on and adjacent to the lower level wiring layer;

forming an upper level wiring layer above the lower level interlayer dielectric layer, wherein the lower level wiring layer is electrically connected to the upper level wiring layer;

forming a protective insulation layer on the upper level wiring layer;

removing a first portion of the protective insulation layer over the upper level wiring layer and over the lower level interlayer dielectric layer to form a pad opening section of the upper level wiring layer,

wherein a second portion of the protective insulation layer located vertically above the lower level wiring layer remains after removing the first portion of the protective layer; and

wherein no portion of the lower level wiring layer is disposed vertically below the pad opening section.

18. A method as in claim 17, further comprising forming an intermediate wiring layer and an intermediate interlayer dielectric layer; wherein the intermediate wiring layer is positioned above the lower level wiring layer and below the upper level wiring layer; and the intermediate interlayer dielectric layer is positioned above the lower level interlayer dielectric layer and below the upper level wiring layer.

19. A method as in claim 18, wherein no portion of the intermediate lower level wiring layer is disposed vertically below the pad opening section.

20. A method as in claim 18, further comprising:

forming the lower level wiring layer to be electrically connected to the intermediate level wiring layer;

forming the intermediate level wiring layer to be electrically connected to the upper level wiring layer;

forming the lower level wiring layer to include has a thickness that is less than that of the lower level interlayer dielectric layer;

forming the intermediate level wiring layer to include a thickness that is less than that of the intermediate level interlayer dielectric layer;

forming a plurality of lower level plugs to electrically connect the lower level wiring layer to the intermediate level wiring layer;

forming a plurality of intermediate level plugs to electrically connect the intermediate level wiring layer to the upper level wiring layer; and

wherein the intermediate plugs are formed to be offset from the lower level intermediate plugs in a vertical direction.

21. A method as in claim 17, further comprising forming a reflection prevention film on the upper level wiring layer.

22. A method as in claim 21, further comprising removing the reflection prevention film from the pad opening section of the upper level wiring layer.

23. A device as in claim 5, further comprising a reflection prevention film formed on the second wiring layer.

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